What is claimed is:

1. A semiconductor device having multiple wiring layers, comprising:

a signal line which is formed in a wiring layer, and to which a signal voltage is applied;

two adjacent lines which are so adjacent to said signal line as not to be connected thereto, and which are formed in a wiring layer where said signal line is formed;

two intersection lines which are respectively formed in wiring layers each being present via an insulating layer above or under the wiring layer where said signal line and said adjacent lines are formed, and which are formed along a surface area corresponding to an area which is enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through the insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines and said two intersection lines.

2. The semiconductor device according to claim 1, wherein said two adjacent lines are formed substantially in parallel to said signal line.

3. The semiconductor device according to claim 1, wherein electric potentials of said two adjacent lines, two intersection lines and entire-line-area through-holes are retained at a predetermined value.

4. The semiconductor device according to claim 1, the electric potentials of said two adjacent lines, said two intersection lines and said entire-line-area through-hole have a same phase as a phase of an electric potential of said signal line.

5. A semiconductor device having multiple wiring layers, comprising:

a plurality of signal lines which are formed not to intersect each other in an identical wiring layer, and to which signal voltages having a same phase are applied;

two adjacent lines which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer

where said plurality of signal lines are formed;

two intersection lines which are formed in a wiring layer each being present via insulating layers above or under the wiring layer where said plurality of signal lines and said two adjacent lines are formed, and which are formed along a surface area corresponding to an area enclosed by said two adjacent lines; and

a plurality of entire-line-area through-holes which respectively penetrate through insulating layers formed between said adjacent lines and said two intersection lines, along entire areas of said two adjacent lines, and which respectively and electrically connect said two adjacent lines with said two intersection lines.

6. The semiconductor device according to claim 5, wherein electric potentials of said two adjacent lines, two intersection lines and entire-line-area through-holes are retained at a predetermined value.

7. The semiconductor device according to claim 6, wherein the electric potentials of said two adjacent lines, two intersection lines and entire-line-area through-holes have a same phase as a phase of an electric potential of said signal lines.

8. A semiconductor device having multiple wiring layers, said device comprising:

a plurality of signal lines which are formed not to intersect each other in an identical wiring layer, and to which signal voltage having different phases are applied;

two first adjacent lines which are so formed adjacent respectively onto outer two of said plurality of signal lines as not to be connected thereto, and which are formed in the wiring layer where said plurality of signal lines are formed;

at least one second adjacent line which is formed in the wiring layer where said plurality of signal lines are formed, between said plurality of signal lines so as not to be connected to said plurality of signal lines;

two intersection lines each of which is formed in a wiring layer being present via an insulating layer above or under the wiring layer where said signal lines and said first

adjacent lines are formed, and each of which is arranged along a surface area corresponding to an area enclosed by said two first adjacent lines; and

entire-line-area through-holes which respectively penetrate through insulating layers formed between said first and second adjacent lines and said two intersection lines along entire areas of said first and second adjacent lines, and which respectively and electrically connect said first and second adjacent lines with said two intersection lines.

9. The semiconductor device according to claim 7, wherein electric potentials of said first and second adjacent lines, two intersection lines and entire-line-area through-holes are retained at a predetermined value.

10. A semiconductor device having multiple wiring layers, said device comprising:

a plurality of signal lines which are formed substantially in parallel to each other in different wiring layers and to which signals having a same phase are respectively applied;

a plurality of adjacent lines each pair of which are so formed adjacent onto both sides of said plurality of signal lines as not to be connected thereto in the wiring layers where said plurality of signal lines are formed;

two intersection lines each of which is formed in a layer under a lowermost wiring layer where said plurality of signal lines are formed or in a layer above an uppermost wiring layer where said plurality of signal lines are formed, and which are formed along a surface area corresponding to an area enclosed by said plurality of adjacent lines formed on the both extreme sides of said plurality of signal lines;

a plurality of first entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines and said two intersection lines, along entire areas of said adjacent lines, and which electrically connect said adjacent lines with said two intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through an insulating layer arranged between said adjacent lines, along the entire areas of said

adjacent lines, and which electrically connects said adjacent lines with each other.

11. The semiconductor device according to claim 10, wherein electric potentials of said adjacent lines, two intersection lines and one or more first and second entire-line-area through-holes are retained at a predetermined value.

12. The semiconductor device according to claim 11, wherein the electric potentials of said adjacent lines, two intersection lines and one or more first and second entire-line-area through-holes have a same phase as a phase of an electric potential of said signal lines.

13. A semiconductor device having multiple wiring layers, said device comprising:

a plurality of signal lines which are formed in different wiring layers, and to which signal voltages are respectively applied;

a plurality of adjacent lines each pair of which are formed either in a lowermost or uppermost wiring layer, of the wiring layers where said plurality of signal lines are formed, respectively adjacent onto both sides of one of said plurality of signal lines which is formed in an identical layer, thereby not to be connected to the one of said plurality of signal lines;

two first intersection lines, each of which is formed either in a wiring layer under the lowermost wiring layer of said signal lines, or in a wiring layer above the uppermost wiring layer of said signal lines, and each of which is formed along a surface area corresponding to an area enclosed by said pair of adjacent lines formed on the both sides of a corresponding one of said plurality of signal lines formed either in the lowermost or uppermost wiring layer of said signal lines;

a second intersection line which is formed in a wiring layer formed between said wiring layers of said signal lines, and which is formed along a surface area corresponding to at least one area enclosed by said pair of adjacent lines;

a plurality of first entire-line-area through-holes which penetrate through insulating

layers respectively formed between said adjacent lines and said first intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said two first intersection lines; and

a plurality of second entire-line-area through-holes which penetrate through insulating layers respectively formed between said adjacent lines and said second intersection lines, along entire areas of said adjacent lines, thereby electrically connecting said adjacent lines with said second intersection line.

14. The semiconductor device according to claim 13, wherein signal voltages which are out of phase are respectively applied to said plurality of signal lines.

15. The semiconductor device according to claim 14, wherein electric potentials of said first and second adjacent lines, first and second intersection lines and first and second entire-line-area through-holes have a same phase as an electric potential of said signal lines.

16. The semiconductor device according to claim 13, wherein said signal lines formed in different layers which are adjacent to each other intersect each other.

17. A semiconductor device having a structure in which a signal line, to which a signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, whose electric potentials are set at a predetermined value.

18. A semiconductor device having a structure in which a signal line, to which a signal voltage is applied, is entirely enclosed by one or more conductors or semiconductors, to which a voltage whose electric potential has a same phase as a phase of said signal line is applied.